REMARKS

In the Office Action, the Examiner noted that Claims 1-34 are pending in the application and that Claims 1-3, 5-11, 13-26, and 28-34 are rejected. The Examiner objected to Claims 4, 12, and 27. By this response, Claims 31 and 33 are amended. In view of the above amendments and the following discussion, Applicants submit that none of the claims now pending in the application are anticipated under the provisions of 35 U.S.C. §102 or obvious under the provisions of 35 U.S.C. §103. Thus, Applicants believe that all of these claims are now in condition for allowance.

I. Objections

A. Drawings

The Examiner objected to the drawings, in particular, FIG. 2. The Examiner noted that the referred element "path 2" in FIG. 2 is specified in the specification as "path 3." Applicants submit herewith a corrected drawing sheet in compliance with 37 C.F.R. §1.121 that replaces the reference element "path 2" with the reference element "path 3" in FIG. 2. Amended FIG. 2 is now consistent with the specification and no new matter has been entered. Accordingly, Applicants respectfully request that the objection to the drawings be withdrawn.

B. Claims

The Examiner objected to claims 31 and 33 as having elements that lack antecedent basis. In particular, the term "the computer automated tool" recited therein lacks antecedent basis. Applicants have amended claims 31 and 33 to delete the term "the computer automated tool." Accordingly, Applicants respectfully request that the objection to claims 31 and 33 be withdrawn.

The Examiner has also objected to dependent claims 4, 12, and 27 as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form. Applicants thank the Examiner for indicating allowable subject matter, but believe independent claims 1, 9, and 24, from which these dependent claims depend, are allowable over the prior art of record for the reasons set forth below. Thus, Applicants contend that claims 4, 12, and 27 should distinguish over the

prior art of record, since each claim depends from independent claims 1, 9, or 24. Therefore, Applicants respectfully request that the objection to claims 4, 12, and 27 be withdrawn.

II. Rejection of Claims Under 35 U.S.C. §102

The Examiner rejected claims 1 and 5-6 as being anticipated by Betz (United States patent 6,763,506, issued July 13, 2004). The rejection is respectfully traversed.

More specifically, the Examiner stated that Betz discloses a method of estimating an upper-bound for an operational frequency of at least a portion of a placed circuit design. (Office Action, p. 3). Notably, the Examiner stated that Betz teaches the steps of determining a minimum path slack corresponding to each connection of a clock domain, selecting the connections based on minimum path slack, and routing one or more of the selected connections in delay mode. (Office Action, p. 3). Applicants respectfully disagree.

Betz generally teaches optimization of a circuit design having multiple timing constraints. (See Betz, Abstract). In particular, Betz discloses receiving a design having various connections between various blocks. Each of the connections forms part of one or more paths through at least a portion of the design, and each path has an associated timing constraint. (Betz, Abstract). The blocks are randomly placed on a target device, routing between the blocks is estimated, and delays associated with the routings are obtained. In response to the delays, the timing constraints for various connections may be relaxed if an associated path has negative slack. (Betz, col. 11, 38-65; FIG. 5). Criticality for each routing connection is then computed and selected blocks are moved followed by a recalculation of the estimated routing and delay connections to and from the moved blocks. (Betz, col. 13, lines 24-65; FIG. 5).

Betz, however, does not teach each and every element of Applicants' invention recited in claim 1. Namely, Betz does not teach or suggest "selecting the connections based on minimum path slack" and "routing one or more of the selected connections in delay mode." (See Applicants' claim 1). First, the Examiner cited step 612 of FIG. 6A in Betz and its corresponding description in column 12, lines 1-42 as disclosing the step of "selecting the connections based on minimum path slack" in Applicants' claim

1. However, in step 612 of Betz, each of the paths in the design is selected until there are no more paths to be evaluated. (Betz, col. 12, lines 15-23). The paths of the design are not selected at step 612 in Betz based on minimum path slack. Betz does not teach or suggest selecting connections based on minimum path slack.

Second, Betz does not teach or suggest routing the selected connections in delay mode. Rather, Betz teaches moving selected logic blocks after computing criticalities of routing connections. That is, in Betz, the logic blocks are selected and placements of the selected logic blocks within the target device are modified. This is in contrast to Applicants' claim 1, where initially routed connections are selected based on minimum path slack and one or more of the selected connections are routed in delay mode. The placement of logic in Applicants' claim 1does not change. Changing the placement of selected logic blocks, as disclosed in Betz, does not teach or suggest routing one or more selected connections in delay mode, as recited in Applicants' claim 1. Betz is devoid of any teaching or suggestion of changing routing of specific connections selected based on minimum path slack.

"Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim." Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 221 USPQ 481, 485 (Fed. Cir. 1984). Since Betz does not teach or suggest selecting the connections based on minimum path slack and then routing one or more of the selected connections in delay mode, Betz does not teach each and every element of Applicants' claim 1. Claims 5-6 depend, either directly or indirectly, from claim 1 and recite additional features therefor. Since Betz does not anticipate Applicants' invention as recited in claim 1, dependent claims 5-6 are also not anticipated and are allowable. Therefore, Applicants contend that claims 1 and 5-6 are not anticipated by Betz and, as such, fully satisfy the requirements of 35 U.S.C. §102.

III. Rejection Of Claims Under 35 U.S.C. §103

A. Claim 7

The Examiner rejected claim 7 as being unpatentable over Betz in view of Noll (United States patent 6,058,252, issued May 2, 2000). The rejection is respectfully

traversed.

More specifically, the Examiner conceded that Betz does not disclose populating a data structure with the connections of a clock domain and sorting the connections according to the path slack of each connection. (Office Action, p. 4). The Examiner stated, however, that Noll teaches organizing connections in a data structure and sorting the connections in order of increasing slack. (Office Action, p. 4). The Examiner concluded that it would have been obvious to modify the process in Betz with the sorting process of Noll and thereby render obvious Applicants' claim 7.

Noll generally teaches the generation of layout constraints for a circuit design. (Noll, Abstract). In particular, Noll teaches selecting specified circuit elements, identifying a most critical path through each of the specified circuit elements and generating circuit layout constraints from the most critical path. (Noll, Abstract).

Claim 7 depends from claim 1 and recites additional features therefor. The cited references, either singly or in any permissible combination, do not teach, suggest, or otherwise render obvious Applicants' invention recited in claim 1. Namely, the combination of Betz and Noll does not teach or suggest "selecting the connections based on minimum path slack" and "routing one or more of the selected connections in delay mode." (See Applicants' claim 1). First, as discussed above, Betz is devoid of any teaching or suggestion of changing routing of specific connections selected based on minimum path slack. Betz discloses changing the placement of selected logic blocks, rather than connections selected based on minimum path slack. Second, Noll is devoid of any teaching or suggestion of determining an initial routing of connections in a clock domain, selecting connections based on minimum path slack, and routing one or more of the selected connections in delay mode. Rather, Noll is concerned with generating layout constraints for a most critical path in a design.

Accordingly, since neither Betz nor Noll teaches or suggests each and every element of Applicants' claim 1, no conceivable combination of Betz and Noll renders obvious Applicants' claim 1. Therefore, Applicants contend that claim 7, which depends from claim 1, is patentable over the combination of Betz and Noll and, as such, fully satisfies the requirements of 35 U.S.C. §103.

B. Claims 2-3, 8-11, 13-26, and 28-34

The Examiner rejected claims 2-3, 8-11, 13-26, and 28-34 as being unpatentable over Betz in view of Bennett (United States patent 5,659,484, issued August 19, 1997). The rejection is respectfully traversed.

More specifically, the Examiner conceded that Betz does not disclose marking the connections of the clock domain which have a lowest minimum path slack and identifying marked connections that are not routed in delay mode as selected. (Office Action, p. 4). The Examiner stated, however, that Bennett teaches enumerating the connections having a lowest minimum path slack and identifying marked connections that are not routed in delay mode. (Office Action, p. 4). The Examiner concluded that it would have been obvious to modify Betz with the path enumeration process of Bennett.

Bennett generally teaches a frequency driven layout method for FPGAs. (See Bennett, Abstract). In particular, Bennett teaches allowing a circuit designer to specify desired operating frequencies of clock signals in a design and automatically generating a physical layout that will allow the FPGA to operate at the specified frequencies. (Bennett, Abstract).

First, claims 2-3 and 8 depend from claim 1 and recite additional features therefor. The cited references, either singly or in any permissible combination, do not teach, suggest, or otherwise render obvious Applicants' invention recited in claim 1. Namely, the combination of Betz and Bennett does not teach or suggest "selecting the connections based on minimum path slack" and "routing one or more of the selected connections in delay mode." (See Applicants' claim 1). First, as discussed above, Betz is devoid of any teaching or suggestion of changing routing of specific connections selected based on minimum path slack. Rather, Betz disclose changing the placement of selected logic blocks. Second, Bennett is devoid of any teaching or suggestion of determining an initial routing of connections in a clock domain, selecting connections based on minimum path slack, and routing one or more of the selected connections in delay mode. Since neither Betz nor Bennett teaches or suggests each and every element of Applicants' claim 1, no conceivable combination of Betz and Bennett renders obvious Applicants' claim 1. Accordingly, claims 2-3 and 8, which depend from claim 1, are nonobvious in view of Betz and Bennett.

Second, the cited references, either singly or in any permissible combination, do not teach, suggest, or otherwise render obvious Applicants' invention recited in claim 9. Namely, the combination of Betz and Bennett does not teach or suggest "constraining at least two clock sources within the placed circuit design to a same target frequency, wherein each clock source is associated with a different clock domain." Bennett does not teach or suggest constraining multiple clock sources in a placed circuit design to a same target frequency. Betz teaches that a multiplication factor between clocks is maintained when a timing constraint is relaxed on a clock. (Betz, col. 12, lines 6-14). Note that the clocks in Betz have different frequencies. Maintaining a multiplication factor between clocks does not teach or suggest constraining at least two clock sources to a same target frequency.

In addition, the combination of Betz and Bennett does not teach or suggest "identifying marked connections which are not routed in delay mode" and "routing one or more of the identified connections in delay mode." Betz does not teach or suggest such features. The routing process of Bennett focuses solely on path delay and timing constraints. Bennett does not teach or suggest identifying connections that are not routed in delay mode and then routing connections in delay mode. That is, Bennett does not distinguish between modes of routing connections. Thus, neither reference teaches or suggests identifying connections that are not routed in delay mode and then routing connections in delay mode.

Since neither Betz nor Bennett teach or suggest each and every element of Applicants' claim 9, no conceivable combination of Betz and Bennett renders obvious Applicants' claim 9. Independent claims 16 and 31 recite, among other features, identifying marked connections which are not routed in delay mode and routing one or more of the identified connections in delay mode. For the reasons set forth above, the combination of Betz and Bennett does not render obvious claims 16 and 31. Independent claims 24 and 33 recite, among other features, constraining at least two clock sources within a placed design to a same target frequency, identifying marked connections that are not routed in delay mode, and routing one or more of the identified connections in delay mode. For the reasons set forth above, the combination of Betz and Bennett also fails to render obvious claims 24 and 33.

Finally, claims 10-11, 13-15, 17-23, 25-26, and 28-30, 32, and 34 depend, either directly or indirectly, from claims 9, 16, 24, 31, and 33 and recite additional features therefor. Since the combination of cited references does not render obvious Applicants' invention as recited in claims 9, 16, 24, 31, and 33, dependent claims 10-11, 13-15, 17-23, 25-26, and 28-30, 32, and 34 are also nonobvious and are allowable.

Therefore, Applicants contend that claims 2-3, 8-11, 13-26, and 28-34 are patentable over the combination of cited references and, as such, fully satisfy the requirements of 35 U.S.C. §103.

C. Claims 15, 22, and 30

The Examiner rejected claims 15, 22, and 30 as being unpatentable over Betz in view of Bennett and in further view of Noll. The rejection is respectfully traversed.

Claims 15, 22, and 30 respectively depend from claims 9, 16, and 24 and recite additional features therefor. As discussed above in section III.B, neither Betz nor Bennett teaches or suggests constraining at least two clock sources within a placed design to a same target frequency, identifying marked connections that are not routed in delay mode, and routing one or more of the identified connections in delay mode. Likewise, Noll is devoid of any teaching or suggestion of constraining clock sources to a same target frequency and distinguishing between modes of routing connections, namely, whether the connections are routed in delay mode or some other mode. As such, no conceivable combination of the cited references renders obvious Applicants' invention recited in claims 9, 16, and 24. Therefore, Applicants contend that claims 15, 22, and 30, which respectively depend from claims 9, 16, and 24, are patentable over the cited references and, as such, fully satisfy the requirements of 35 U.S.C. §103.

CONCLUSION

Thus, Applicants submit that none of the claims presently in the application are anticipated under the provisions of 35 U.S.C. §102 or obvious under the provisions of 35 U.S.C. §103. Consequently, Applicants believe that all these claims are presently

in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If, however, the Examiner believes that there are any unresolved issues requiring any adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Kim Kanzaki at (408) 879-6149 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

Respectfully submitted,

Kim Kanzaki, Ph.D.
Attorney for Applicants
Reg. No. 37,652

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on October 25, 2005.

Pat Tompkins
Name

Pat Tompkins
Signature

AMENDMENTS TO THE DRAWINGS

Applicants submit a Replacement Sheet for FIG. 2. Amended FIG. 2 is now consistent with the specification and no new matter has been entered.